

In the Claims

Please amend the claims as follows:

Claims 1 to 43 (Canceled)

B1

1 44. (Currently Amended) A single integrated circuit
2 comprising:
3 a first data processor including
4 a first program counter (2903) storing an address of a
5 next instruction,
6 a first opcode register (2911) storing a current
7 instruction,
8 first data processing units (2902, 2905, 2906, 2907,
9 2908, 2909, 2910) capable of data processing,
10 a first control logic (2904) connected to said opcode
11 register for control of said first data processing units
12 corresponding to said current instruction stored in said first
13 opcode register according to a first instruction set;
14 a second data processor including
15 a second program counter (3100) storing an address of a
16 next instruction,
17 a second opcode register (3105) storing a current
18 instruction,
19 second data processing units (3301, 3302, 3303, 3304)
20 capable of data processing,
21 a second control logic (3002) connected to said opcode
22 register for control of said second data processing units
23 corresponding said current instruction stored in said second
24 opcode register according to a second instruction set, said
25 second ~~instruction set~~ data processing units having a

26 different mapping of instructions to controlled operations
27 than that of said first instruction set; and
28 an external interface (11) connected to said first and second
29 data processors and adapted for connection to memory (15) external
30 to said single integrated circuit, said external interface forming
31 the only connection between said first and second data processors
32 and memory external to said single integrated circuit;
33 where said first and second data processors are capable of
34 independent operations on disjoint instructions and data sets.

Claim 45. (Canceled)

1 46. (Previously Added) The single integrated circuit of claim
2 44, wherein:

3 said first data processor further includes a first data
4 register file (2901) connected to said first data processing units
5 for temporarily storing data; and

6 said second data processor further includes a second data
7 register file (3300) connected to said second data processing units
8 for temporarily storing data.

1 47. (Currently Amended) The single integrated circuit of
2 claim 44, further comprising:

3 a first read/write memory connected to said first data
4 processor and to said second data processor, whereby said first
5 processor ~~is~~ and said second data processor are each capable of
6 reading from ~~or~~ and writing to said first read/write memory; and

7 a second read/write memory connected to said second data
8 processor, whereby said second data processor is capable of reading
9 from ~~or~~ and writing to said second read/write memory and said first
10 data processor is not capable of either reading from or writing to
11 said second read/write memory.

B/ Claim 48. (Canceled)

1 49. (Previously Added) The single integrated circuit of claim
2 44, wherein:
3 said first data processor is a digital signal processor (DSP);
4 and
5 said second data processor is a reduced instruction set
6 computer (RISC) processor.

Claims 50 and 51. (Canceled)

1 52. (Currently Amended) A single integrated circuit
2 comprising:
3 a first data processor including
4 a first program counter (2903) storing an address of a
5 next instruction,
6 a first opcode register (2911) storing a current
7 instruction,
8 first data processing units (2902, 2905, 2906, 2907,
9 2908, 2909, 2910) capable of data processing,
10 a first control logic (2904) connected to said opcode
11 register for control of said first data processing units
12 corresponding to said current instruction stored in said first
13 opcode register according to a first instruction set;
14 a first read/write memory connected to said first data
15 processor, whereby said first processor is capable of reading from
16 ~~or~~ and writing to said first read/write memory;
17 a first instruction memory connected to said first data
18 processor storing instructions in said first instruction set, said
19 first data processor operating in accordance with instructions in
20 said first instruction set recalled from said first instruction
21 memory;

22 B\ a second data processor including
23 a second program counter (3100) storing an address of a
24 next instruction,
25 a second opcode register (3105) storing a current
26 instruction,
27 second data processing units (3301, 3302, 3303, 3304)
28 capable of data processing,
29 a second control logic (3002) connected to said opcode
30 register for control of said second data processing units
31 corresponding said current instruction stored in said second
32 opcode register according to a second instruction set, said
33 second ~~instruction set~~ data processing units having a
34 different mapping of instructions to controlled operations
35 than that of said first instruction set;
36 a second read/write memory connected to said second data
37 processor, whereby said second processor is capable of reading from
38 ~~or~~ and writing to said second read/write memory;
39 a second instruction memory connected to said second data
40 processor storing instructions in said second instruction set, ~~said~~
41 said second processor operating in accordance with instructions in
42 said second instruction set recalled from said second instruction
43 memory; and
44 an external interface (11) connected to said first and second
45 data processors and connectable to ~~devices~~ memory (15) external to
46 said single integrated circuit, said external interface forming the
47 only connection between said first and second data processors and
48 memory external to said single integrated circuit;
49 where said first and second data processors are capable of
50 independent operations on disjoint instructions and data sets.

1 53. (Previously Added) The single integrated circuit of claim
2 52, wherein:

B1
3 said first data processor further includes a first data
4 register file (2901) connected to said first data processing units
5 for temporarily storing data; and

6 said second data processor further includes a second data
7 register file (3300) connected to said second data processing units
8 for temporarily storing data.

1 54. (Previously Added) The single integrated circuit of claim
2 52, wherein:

3 said first data processor is a digital signal processor (DSP);
4 and

5 said second data processor is a reduced instruction set
6 computer (RISC) processor.

Claims 55 and 56. (Canceled)

B2
1 57. (New) The single integrated circuit of claim 47, wherein:
2 said first data processor is operable to generate a request
3 for data movement to or from said first read/write memory;

4 said second data processor is operable to generate a request
5 for data movement to or from said first read/write memory and for
6 data movement to or from said second read/write memory;

7 said external interface is operable to receive a request for
8 data movement from said first data processor and from said second
9 data processor and to move data responsive thereto.

1 58. (New) The single integrated circuit of claim 57, wherein:
2 each request for data movement generated by said first data
3 processor or generated by said second data processor includes an
4 indication of source address, an indication of destination address
5 and an indication of amount of data; and

6 said external interface is operable upon receipt of said
7 request for data movement to move said indicated amount of data
8 from said indicated source address to said indicated destination
9 address.

B2
1 59. (New) The single integrated circuit of claim 57, wherein:
2 said first read/write memory is operable to prioritize
3 requests for access with said first data processor having a highest
4 priority, said second data processor having an intermediate
5 priority and said external interface having a lowest priority.

1 60. (New) The single integrated circuit of claim 52, wherein:
2 said first data processor is operable to generate a request
3 for data movement to or from said first read/write memory;
4 said second data processor is operable to generate a request
5 for data movement to or from said first read/write memory and for
6 data movement to or from said second read/write memory;
7 said external interface is operable to receive a request for
8 data movement from said first data processor and from said second
9 data processor and to move data responsive thereto.

1 61. (New) The single integrated circuit of claim 60, wherein:
2 each request for data movement generated by said first data
3 processor or generated by said second data processor includes an
4 indication of source address, an indication of destination address
5 and an indication of amount of data; and
6 said external interface is operable upon receipt of said
7 request for data movement to move said indicated amount of data
8 from said indicated source address to said indicated destination
9 address.

1 62. (New) The single integrated circuit of claim 57, wherein:

2 said first read/write memory is operable to prioritize
3 requests for access with said first data processor having a highest
4 priority, said second data processor having an intermediate
5 priority and said external interface having a lowest priority.

1 63. (New) A single integrated circuit comprising:

2 a first data processor including

B2 3 a first program counter (2903) storing an address of a
4 next instruction,

5 a first opcode register (2911) storing a current
6 instruction,

7 first data processing units (2902, 2905, 2906, 2907,
8 2908, 2909, 2910) capable of data processing,

9 a first control logic (2904) connected to said opcode
10 register for control of said first data processing units
11 corresponding to said current instruction stored in said first
12 opcode register according to a first instruction set;

13 a second data processor including

14 a second program counter (3100) storing an address of a
15 next instruction,

16 a second opcode register (3105) storing a current
17 instruction,

18 second data processing units (3301, 3302, 3303, 3304)
19 capable of data processing,

20 a second control logic (3002) connected to said opcode
21 register for control of said second data processing units
22 corresponding said current instruction stored in said second
23 opcode register according to a second instruction set, said
24 second instruction set units having a different mapping of
25 instructions to controlled operations than that of said first
26 instruction set;

B2 27 a read/write memory connected to said first data processor and
28 said second data processor whereby both said first data processor
29 and said second data processor are each capable of reading from and
30 writing to said read/write memory;

31 an external interface (11) connected to said first data
32 processor, said second data processors and adapted for connection
33 to memory (15) external to said single integrated circuit, said
34 external interface forming the only connection between said first
35 data processor and said second data processors and memory external
36 to said single integrated circuit, wherein said first data
37 processor and said second data processor are each capable of
38 generating a request for data movement to or from said read/write
39 memory and said external interface is operable to receive a request
40 for data movement from said first data processor and from said
41 second data processor and to move data responsive thereto; and

42 wherein said first and second data processors are capable of
43 independent operations on disjoint instructions and data sets.

1 64. (New) The single integrated circuit of claim 63, wherein:
2 said first data processor further includes a first data
3 register file (2901) connected to said first data processing units
4 for temporarily storing data; and
5 said second data processor further includes a second data
6 register file (3300) connected to said second data processing units
7 for temporarily storing data.

1 65. (New) The single integrated circuit of claim 63, wherein:
2 each request for data movement generated by said first data
3 processor or generated by said second data processor includes an
4 indication of source address, an indication of destination address
5 and an indication of amount of data; and

6 said external interface is operable upon receipt of said
7 request for data movement to move said indicated amount of data
8 from said indicated source address to said indicated destination
9 address.

1 66. (New) The single integrated circuit of claim 63, wherein:
2 said read/write memory is operable to prioritize requests for
3 access with said first data processor having a highest priority,
4 said second data processor having an intermediate priority and said
5 external interface having a lowest priority.

1 67. (New) The single integrated circuit of claim 63, further
2 comprising:
3 a second read/write memory connected to said second data
4 processor, whereby said second data processor is capable of reading
5 from and writing to said second read/write memory and said first
6 data processor is not capable of either reading from or writing to
7 said second read/write memory.

1 68. (New) The single integrated circuit of claim 63, wherein:
2 said first data processor is a digital signal processor (DSP);
3 and
4 said second data processor is a reduced instruction set
5 computer (RISC) processor.

1 69. (New) A single integrated circuit comprising:
2 a first data processor including
3 a first program counter (2903) storing an address of a
4 next instruction,
5 a first opcode register (2911) storing a current
6 instruction,

7 first data processing units (2902, 2905, 2906, 2907,
8 2908, 2909, 2910) capable of data processing,
9 *BZ* a first control logic (2904) connected to said opcode
10 register for control of said first data processing units
11 corresponding to said current instruction stored in said first
12 opcode register according to a first instruction set;
13 a first read/write instruction memory connected to said first
14 data processor storing instructions in said first instruction set,
15 said first data processor operating in accordance with instructions
16 in said first instruction set recalled from said first instruction
17 memory;
18 a second data processor including
19 a second program counter (3100) storing an address of a
20 next instruction,
21 a second opcode register (3105) storing a current
22 instruction,
23 second data processing units (3301, 3302, 3303, 3304)
24 capable of data processing,
25 a second control logic (3002) connected to said opcode
26 register for control of said second data processing units
27 corresponding said current instruction stored in said second
28 opcode register according to a second instruction set, said
29 second data processing units having a different mapping of
30 instructions to controlled operations than that of said first
31 instruction set;
32 a second read/write instruction memory connected to said
33 second data processor storing instructions in said second
34 instruction set, said second processor operating in accordance with
35 instructions in said second instruction set recalled from said
36 second instruction memory; and
37 a read/write data memory connected to said first data
38 processor and said second data processor, whereby both said first

39 data processor and said second processor are capable of reading
40 from and writing to said read/write data memory.

B2

1 70. (New) The single integrated circuit of claim 69, wherein:
2 said first data processor further includes a first data
3 register file (2901) connected to said first data processing units
4 for temporarily storing data; and
5 said second data processor further includes a second data
6 register file (3300) connected to said second data processing units
7 for temporarily storing data.

1 71. (New) The single integrated circuit of claim 69, wherein:
2 said read/write data memory is operable to prioritize requests
3 for access with said first data processor having a highest priority
4 and said second data processor having a lowest priority.

1 72. (New) The single integrated circuit of claim 69, further
2 comprising:
3 a second read/write data memory connected to said second data
4 processor, whereby said second data processor is capable of reading
5 from and writing to said second read/write data memory and said
6 first data processor is not capable of either reading from or
7 writing to said second read/write data memory.

1 73. (New) The single integrated circuit of claim 69, wherein:
2 said first data processor is a digital signal processor (DSP);
3 and
4 said second data processor is a reduced instruction set
5 computer (RISC) processor.

1 74. (New) The single integrated circuit of claim 69, wherein:

2 said first and second data processors are capable of
3 independent operations on disjoint instructions and data sets.

B72
1 75. (New) The single integrated circuit of claim 69, wherein:
2 said first read/write instruction memory being configured as a
3 first instruction cache;

4 said second read/write instruction memory being configured as
5 a second instruction cache;

6 said first data processor further including a first
7 instruction cache logic circuit (3101) connected to said program
8 counter and said first instruction cache for determining if an
9 instruction corresponding to the address stored in said first
10 program counter is stored in said first instruction cache;

11 said second data processor further including a second
12 instruction cache logic circuit connected to said second program
13 counter and said second instruction cache for determining if an
14 instruction corresponding to the address stored in said second
15 program counter is stored in said second instruction cache; and.

16 an external interface (11) connected to said first data
17 processor, said second data processor, said first instruction cache
18 and said second instruction cache and connectable to memory (15)
19 external to said single integrated circuit, said external interface
20 transferring an instruction corresponding to the address stored in
21 said first program counter from said memory external to said single
22 integrated circuit to said first instruction cache if said first
23 instruction cache logic circuit determines said instruction is not
24 stored in said first instruction cache, and said external interface
25 transferring an instruction corresponding to the address stored in
26 said second program counter from said memory external to said
27 single integrated circuit to said second instruction cache if said
28 second instruction cache logic circuit determines the instruction
29 is not stored in said second instruction cache.
